PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference W 6874-011 LB	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/EP2005/002221	International filing date *(day/month/year)* 03.03.2005	Priority date *(day/month/year)* 10.03.2004
International Patent Classification (IPC) or national classification and IPC H03M13/27		
Applicant TELEFONAKTIEBOLAGET L M ERICSSON (PUBL) et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 4 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 8 sheets, as follows:
      ☐ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

Date of submission of the demand	Date of completion of this report
25.11.2005	16.03.2006
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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/EP2005/002221

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

   Description, Pages

   1-18 as originally filed

   Claims, Numbers

   1-34 filed with telefax on 14.02.2006

   Drawings, Sheets

   1/4-4/4 as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-34
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-34
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-34
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following document:
D1: D1: US 6 314 534 B1

2 The document D1 is regarded as being the closest prior art to the subject-matter of claims 1, 10, 12 and 25 shows (the references in parentheses applying to this document):

A device and a method for generating an address value for addressing a memory, which is an interleaver or deinterleaver memory which generates a plurality of address fragments and compares only a fraction of the generated address fragments with a maximum allowable value (cf figure 2 and column 3, lines 57-61).

The subject-matter of claims 1, 10, 12 and 25 differs from D1 in that only every other address fragment is compared.

The subject-matter of claims 1, 10, 12 and 25 is therefore new (Article 33(2) PCT).

The problem to be solved by the present invention may be regarded as reduce the computational burden.

The solution to this problem proposed in claims 1, 10, 12 and 25 of the present application is considered as involving an inventive step (Article 33(3) PCT), since none of the other prior art documents indicated that it is sufficient to compare only ever other address fragment.

3 Claims 2-9, 11, 13-24 and 26-34 are dependent on claims 1, 10, 12 and 25 and as such also meet the requirements of the PCT with respect to novelty and inventive step.

CLAIMS

1. A method for generating an address value for addressing a memory (31), which is an interleaver or deinterleaver memory, comprising the step of generating a plurality of address fragments, and comparing only a fraction of the generated address fragments with a maximum allowable value, **characterized** in that:

the step of generating comprises generating a first address fragment for a first address value, and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

the step of comparing comprises comparing only every other address fragment of the plurality of address fragments with the maximum allowable value, whereby the step of comparing comprises comparing the first address fragment with the maximum allowable value.

2. The method according to claim 1, further comprising the steps of:

discarding the compared address fragment if it exceeds the maximum allowable value; and

accepting the compared address fragment otherwise.

3. The method according to any of the previous claims, further comprising the step of:

permuting the generated address fragments,

wherein the address fragments to be compared are permuted prior to the step of comparing.

4. The method according to any of the previous claims, further comprising the step of:

appending at least one bit being the most significant bit(s) to any address fragment or permuted address fragment

5. The method according to any of the previous claims, wherein the compared address fragment is an odd address fragment to which a 1 is to be appended as a most significant bit.

6. The method according to any of the previous claims, wherein an even address fragment is generated in response to discarding or accepting the compared address fragment.

7. The method according to any of the claims 1 to 5, comprising the step of:

generating at least the odd address fragment to be compared and a following even address fragment during a first clock cycle;

if the compared odd address fragment is discarded, outputting the even address fragment during the first clock cycle;

if the compared odd address fragment is accepted, outputting the odd compared address fragment and retaining values of registers of a shift register during the first clock cycle; and

outputting the even address fragment during a second clock cycle following the first clock cycle.

8. The method according to any of the previous claims, comprising the step of:

generating a next odd address fragment; and

inputting the next odd address fragment into registers (120a-120d) of a shift register.

9. The method according to claim 7 or 8, wherein the next even and next odd address fragments are generated by means of a feedback function (g(x)).

10. A method for generating an address value for addressing a memory (31), which is an interleaver or deinterleaver memory, comprising the step of generating a plurality of address fragments, and comparing only a fraction of the generated address fragments, **characterized** in that:

the step of generating comprises generating a first address fragment for a first address value, and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

the step of comparing comprises comparing only every other address fragment of the plurality of address fragments with stored address fragments, which are known to be out of range when permuted, whereby the step of comparing comprises comparing the first address fragment with the stored address fragments.

11. The method according to claim 10, further comprising the step of:

permuting the generated address fragments,

wherein the address fragments to be compared are permuted after the step of comparing.

12. A device (100, 200, 300) for generating address values for addressing a memory (31), which is an interleaver or deinterleaver memory, comprising means (110a-110d, 140a, 140b) for generating a plurality of address fragments, and comparator means (160, 260, 360) adapted to compare only a fraction of the plurality of address fragments with a maximum allowable value **characterized** in that

the means (110a-110d, 140a, 140b) for generating a plurality of address fragments is adapted to generate a first address fragment for a first address value and a

second address fragment, which is consecutive of the first address fragment, for a second address value; and

the comparator means (160, 260, 360) is adapted to compare only every other address fragment of the plurality of address fragments with the maximum allowable value, and thereby to compare the first address fragment with the maximum allowable value.

13. The device according to claim 13 or 14, further comprising selector means (150), which is adapted to discard the compared address fragment if it exceeds the maximum allowable value, and to accept the compared address fragment otherwise.

14. The device according to any of the claims 12 to 13, further comprising permuting means (130a, 130b) adapted to permute the address fragments, the permuting means being provided prior to the comparator means (160, 260, 360).

15. The device according to any of the claims 12 to 14, further comprising toggle means (170) adapted to append at least one bit being the most significant bit(s) to any address fragment, or permuted address fragment, in order to generate the address value.

16. The device according to any of the claims 12 to 15, wherein the compared address fragments are address fragments to which a 1 is to be appended as a most significant bit.

17. The device according to any of the claims 12 to 16, wherein the means (110a-110d, 140a) for generating address fragments is adapted to generate a next even address fragment in response to discarding or accepting the compared address fragment.

18. The device according to any of the claims 12 to 16, wherein the means for generating address fragments comprises:

a shift-register comprising a predetermined number of registers (110a-110d) adapted to generate address fragments to be compared during a first clock cycle,

address fragment calculation means (140) adapted to generate a next even address fragment during the first clock cycle, which is based on the address fragment to be compared;

the selector means (150) is adapted to, if the compared address fragment is discarded, output the even address fragment in response to a first control signal (M) during the first clock cycle, and to output the compared address fragment during the first clock cycle if the compared address fragment is accepted, and to output the even address fragment during a second clock cycle following the first clock cycle; and

the shift register is adapted to retain present values of the registers during the first clock cycle in response to a second control signal (E) if the compared address fragment is accepted.

19. The device according to claim 18, wherein the address fragment calculation unit means (140a, 140b) is adapted to generate a next odd address fragment, based on the even address fragment, and feed back said next odd address fragment to the shift register.

20. The device according to claim 18 or 19, wherein the address fragment calculation means (140a, 140b) is adapted to generate the next even and next odd address fragments by means of a feedback function.

21. The device according to any of the claims 12 to 20, wherein the device (100, 200, 300) is implemented by software comprising readable program means to be run by a processor.

22. The device according to any of the claims 12 to 20, wherein the device (100, 200, 300) is implemented as an application specific integrated circuit.

23. The device according to any of the claims 12 to 20, wherein the device (100, 200, 300) is implemented as a field programmable gate array.

24. The device according to any of the claims 12 to 23, further comprising a shift register adapted to generate a maximum length pseudo noise sequence.

25. A device (100, 200, 300) for generating address values for addressing a memory (31), which is an interleaver or deinterleaver memory, comprising means (110a-110d, 140a, 140b) for generating a plurality of address fragments, and comparator means (160, 260, 360) adapted to compare only a fraction of the plurality of address fragments with a maximum allowable value, **characterized** in that

the means (110a-110d, 140a, 140b) for generating a plurality of address fragments is adapted to generate a first address fragment for a first address value and a second address fragment, which is consecutive of the first address fragment, for a second address value; and

the comparator means (160, 260, 360) is adapted to compare only every other address fragment of the plurality of address fragments with stored address fragments, which are known to be out of range when permuted, and thereby to

compare the first address fragment with stored address fragments.

26. The device according to claim 25, further comprising permuting means (130a, 130b) adapted to permute the address fragments, the permuting means being provided after the comparator means (160, 260, 360).

27. An interleaver for interleaving a block of data, comprising a memory (31), which is an interleaver memory, and a device (100, 200, 300) for generating address values according to any of the claims 11 to 28 for addressing the memory.

28. A deinterleaver for interleaving a block of data, comprising a memory (31), which is a deinterleaver memory, and a device (100, 200, 300) for generating address values according to any of the claims 12 to 26 for addressing the memory.

29. A communication apparatus for communicating data, comprising a memory (31), which is an interleaver memory or a deinterleaver memory, and a device according to any of the claims 12 to 26 for generating address values for addressing the memory.

30. The communication apparatus according to claim 29, wherein the communication apparatus is a mobile radio terminal, a pager, a communicator, an electronic organizer, or a smartphone.

31. The communication apparatus according to claim 29, wherein the communication apparatus is a mobile telephone (1).

32. A communication apparatus for receiving data, comprising a deinterleaver according to claim 28.

33. The communication apparatus according to claim 32, wherein the communication apparatus is a set-top-box, a TV-set, or a mobile television receiver.

34. A software program product embodied on a computer readable medium comprising instructions for carrying out the method according to any of the claims 1 to 11 when said product is run by a processor.